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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,085	08/20/2004	Robert J. Gauthier, Jr.	BUR920040079US1	5084

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EXAMINER	
PATEL, DHARTI HARIDAS	

ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 11/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/711,085	GAUTHIER, JR. ET AL.
	Examiner	Art Unit
	Dharti H. Patel	2836

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11-14* is/are allowed.

6)☐ Claim(s) *1-2,5-6, 8- 10* is/are rejected.

7)☐ Claim(s) *3-4 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities:

Page 9, lines 3, 6, "VINV1OUT" should be – "INV1OUT" to be consistent with the drawings.

Page 9, lines 3, 12, "VINV2OUT" should be – "INV2OUT" to be consistent with the drawings.

Appropriate correction is required.

Claim Objections

2. Claims 1, 8 and 11, line 3, "an FET transistor" should read --- "a FET transistor"

Claim 5 recites the limitation "said resistor" in the second line of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 is objected to as a claim cannot depend from a higher numbered claim. Therefore claim 7 will not be further treated.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over the acknowledged prior art, in view of Wu et al., Patent No. 6,552,886. With respect to claims 1 and 8, applicant's prior art (Fig. 1) teaches a

basic ESD triggered power clamp circuit which comprises a FET transistor 11 having drain and source connections connected across power supply terminals 10a and 10b of an integrated circuit for clamping the voltage at said terminals to a power supply voltage during an ESD event; an RC timing circuit 13 and 14 connected between the power supply terminals which provides a voltage proportional to an ESD voltage for triggering said FET transistor 11 out of conduction following an ESD event; an inverter circuit having a plurality stages 16, 17, 18 connected between said power supply terminals, said inverter circuit having an input connection connected to receive said RC timing circuit voltage, and having an output connected to said FET transistor gate connection as disclosed in the Specification, Page 6, lines 9-11, 17-20 and Page 7, lines 2-3.

However, the prior art fails to teach or suggest a feedback FET having a drain and source connected in series with one stage of said inverter circuit and said power supply terminals, and having a gate connection connected to said FET gate connection, whereby during an ESD event, said feedback FET provides dynamic feedback preventing said gate connection from latching said FET transistor for clamping the voltage on said terminals into a conducting mode when power supply potential is applied across said terminals.

Wu et al. teaches an active VCC-to-VSS electrostatic discharge protection circuit that comprises a feedback transistor 28 having a drain and source connected in series with one stage 34 of said inverter circuit and said power supply terminals VCC as disclosed in Col. 4, line 61 and Fig. 4.

Both teachings are related by being electrostatic discharge protection power clamps for suppressing ESD events. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Wu et al., which teaches a feedback transistor, into the power clamp circuit of the applicant's acknowledged prior art to protect the internal power supplies of an integrated circuit. Also, the feedback transistor increases a divided voltage required to turn on the control gate of the clamping transistor, which in turn reduces latch up events.

With respect to claim 2, Wu et al. teaches an active VCC-to-VSS ESD protection circuit that comprises an inverter circuit comprising first 32, second 34, and third 38 pairs of serially connected inverters implemented as FET transistors (Fig. 3) connected across said power supply terminals VCC and VSS, said pairs of transistors 32, 34, 38 having common gate connections, said first pair of transistors 32 having gate connections connected to said RC timing circuit 24 and 25, said second pair of transistors 34 having gate connections connected to the serial connection of said first pair of transistors 32, and said third pair of transistors 38 having gate connections connected to the serial connection of said second pair of transistors 34, said feedback FET 28 being connected in series with said second pairs of serially connected transistors 34, said third pair of transistors 38 serial connection connected to said FET 30 gate connection as disclosed in Fig. 3 and Fig. 4.

With respect to claim 5, it would have been obvious to those skilled in the art at the time the invention was made to add a FET based resistor for forming an RC circuit comprised of a resistor in combination with the parasitic capacitance of FET to enhance response during transient ESD events.

With respect to claim 6, Wu et al. teaches a feedback transistor 28 that is connected in series with a pull up transistor of said inverter circuit stage 34 as disclosed in Fig. 4.

With respect to claim 9, Wu et al. teaches a polarity which is reversed from the claimed N-MOSFET transistor as a feedback transistor and P-MOSFET transistor as a FET transistor. It would have been obvious to those skilled in the art at the time the invention was made to reverse the polarity of the transistor devices to address the expected polarity of an ESD event or to address polarity considerations related to power supply connections.

With respect to claim 10, Wu et al. teaches an ESD protection circuit wherein the FET transistor 30 is an N-MOSFET transistor and the feedback transistor 28 is a P-MOSFET transistor as disclosed in Fig. 4.

Allowable Subject Matter

4. Claims 3-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for indicating allowance of claim 3: Wu et al. teaches an ESD protection circuit that comprises

an inverter circuit, an RC circuit, and a feedback transistor but does not disclose a second feedback transistor for supplying a feedback signal to said inverter circuit from said FET gate connection for reducing the power up current drawn by said FET during power up. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

5. Claims 11-14 are allowed. The following is an examiner's statement of reasons for indicating allowance of claim 11: Wu et al. teaches an ESD protection circuit that comprises a FET transistor, an RC timing circuit, an inverter circuit connected across power supply terminals VCC and VSS, and a first feedback transistor but does not disclose a second feedback transistor having source and drain connections connected across said serial connection of said first transistor and said pull-up transistor, said second feedback transistor reducing power consumption during a power up of said power supply voltage. This feature in combination with the rest of the claim limitations is not anticipated or rendered obvious by the prior art of record.

6. ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dharti H. Patel whose telephone number is 571-272-8659. The examiner can normally be reached on 8:30am - 5pm.
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on 571-272-2800, Ext. 36. The fax

phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DHP
11/04/2005

PHUONG T. VU
PRIMARY EXAMINER